VLSI DESIGN IN FPGA USING VHDL					
DAY	TOPIC	DESCRIPTION	THEORY	LAB	TOTAL
DAY1	Introduction to VHDL	Purpose and Background of VHDL,Design Synthesis process,Design Tool Flow, VHDL Modeling styles	3HRs	NIL	3HRs
	VHDL Basics and Simulation	Entity Architecture Structure, Code Model, Device Model,Ports and Its Types	30Mins	1Hr	1.5HRs
	Operators and Attributes with Simulation	Logical,Relational,Shift Operators,Arithmetic Operators	30Mins	1Hr	1.5HRs
DAY2	Data Flow Modeling	Concurrent Signal Assignments,Conditional Signal Assignments	30Mins	90Mins	1.5HRs
	Structural Modeling	,Component Declaration,Component Instantiation,General Statement	30Mins	90Mins	1.5HRs
	Simulation Tools	Familiarization of simulation tools like Xilinx, Modelsim	1Hr	2HRs	3HRs
DAY3	Behavioral Modeling	Process,Variables and signals,Conditional and looping statements	30Mins	90Mins	1.5HRs
	Examples	Simulation Examples in xilinx	30Mins	90Mins	1.5HRs
	Synthesis	Programming FPGA, interfacing LED , interfacing switches , interfacing adc	1Hr	2HRs	3HRs

DAY4	UART IP core design	Uart Protocol, baudrate generator design	30Mins	90Mins	1.5HRs
	UART IP core design	UART transmission and reception design	30Mins	90Mins	1.5HRs
	Synthesis	Programming FPGA, and testing UART	1Hr	2HRs	3HRs

DAY5	LCD IP core design	LCD programming in FPGA	30Mins	90Mins	1.5HRs
	Camera interfacing IP core design	capturing picture using FPGA	30Mins	90Mins	1.5HRs
	Image processing using FPGA	Edge detection algorithm implementation	1Hr	2HRs	3HRs